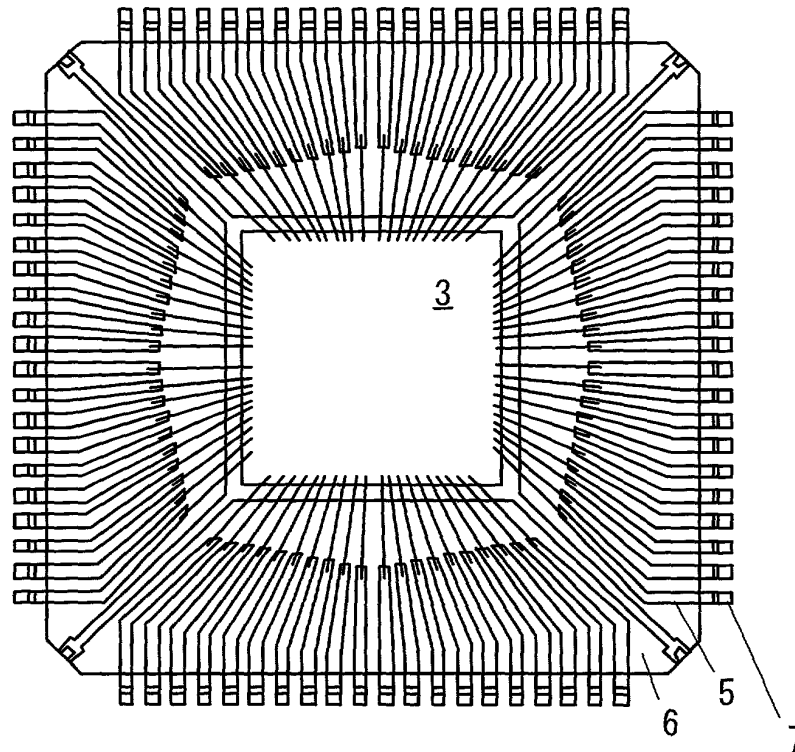
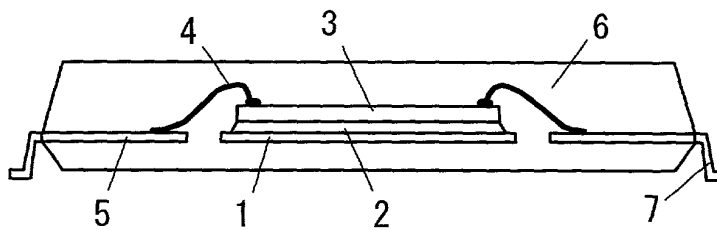


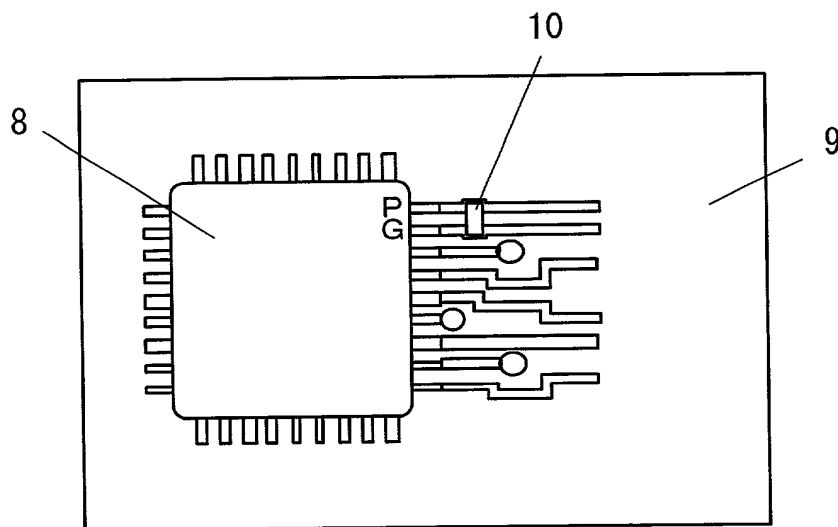
*FIG. 1A*  
*(Prior Art)*

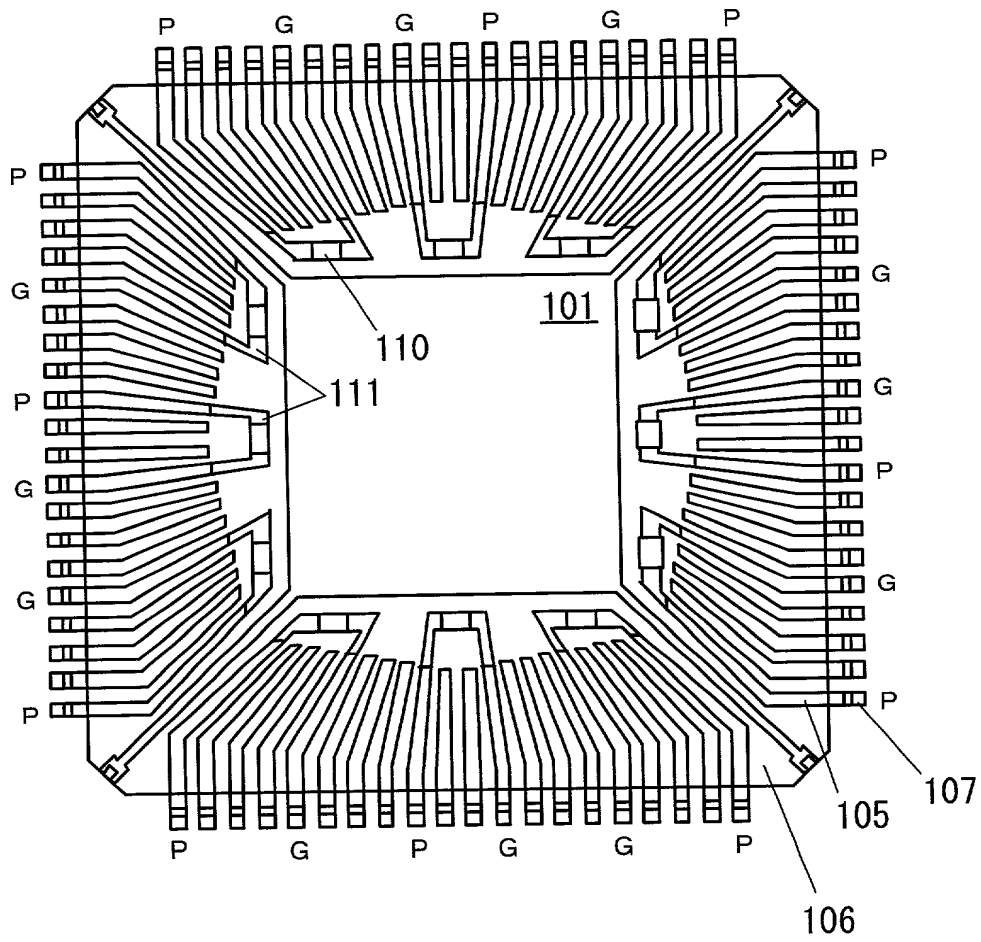


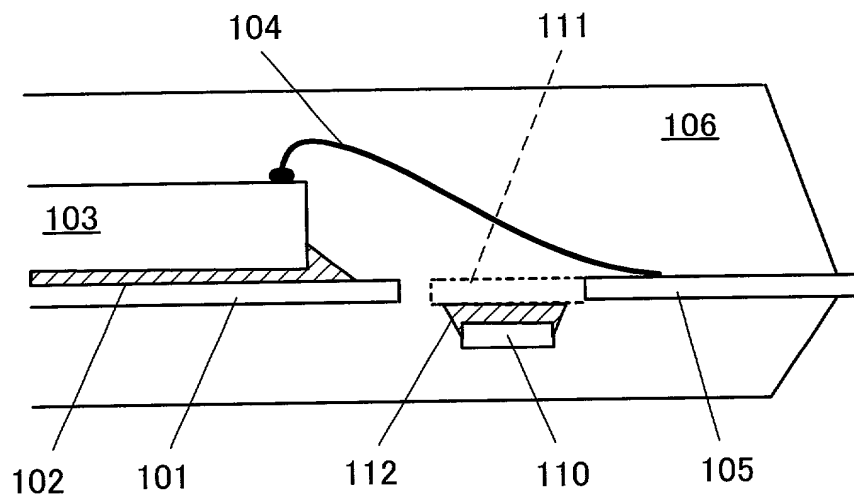
*FIG. 1B*  
*(Prior Art)*

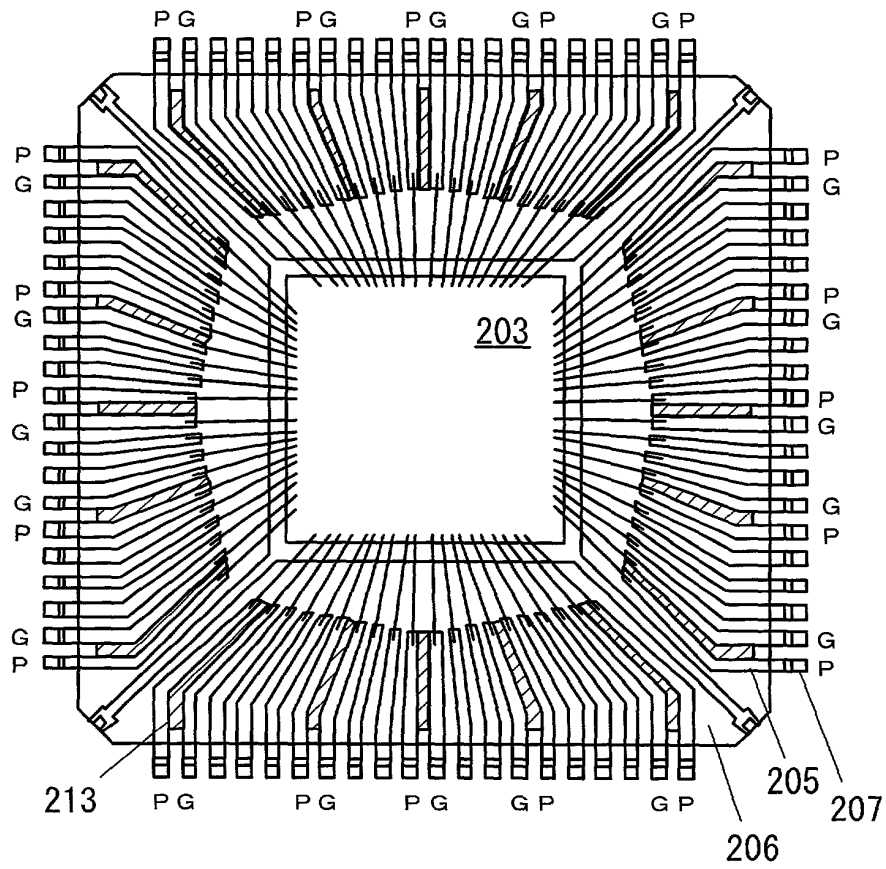


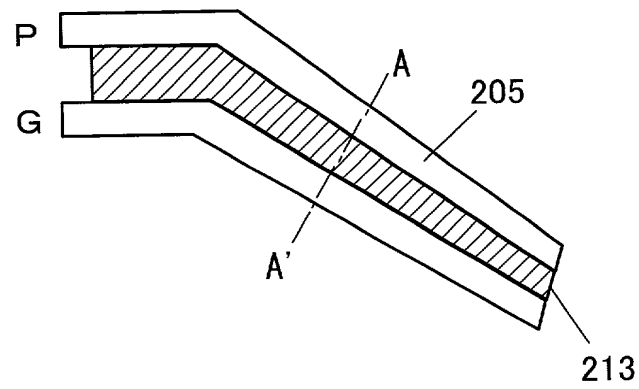
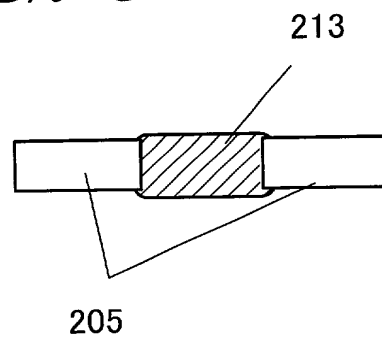
*FIG. 2*  
*(Prior Art)*

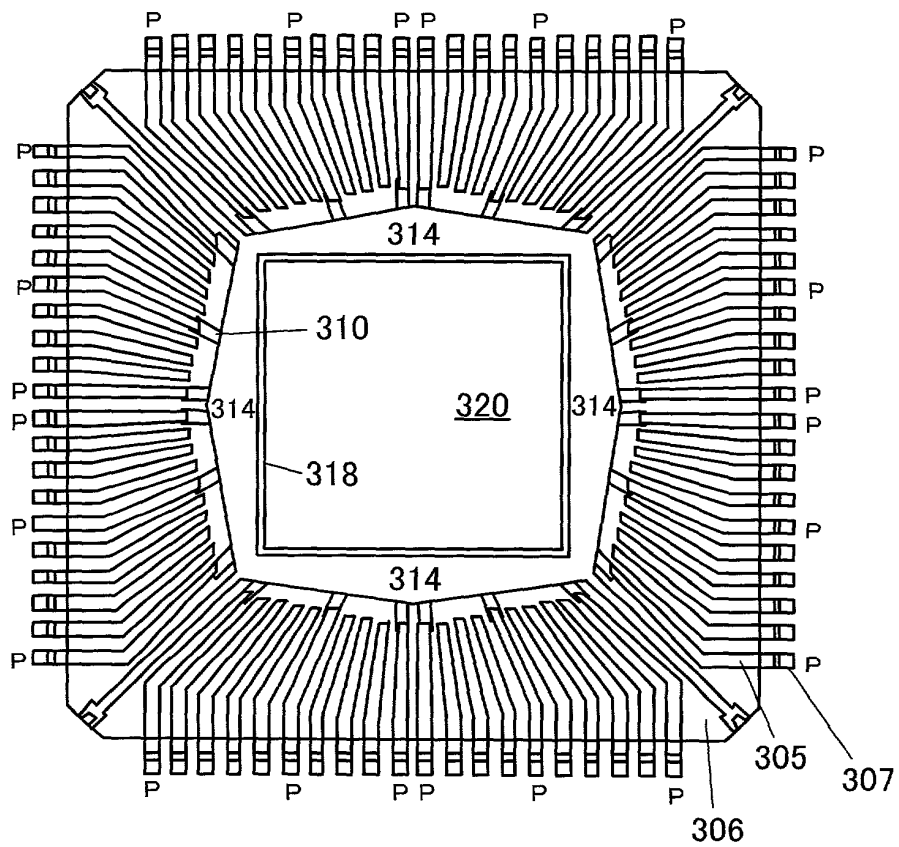


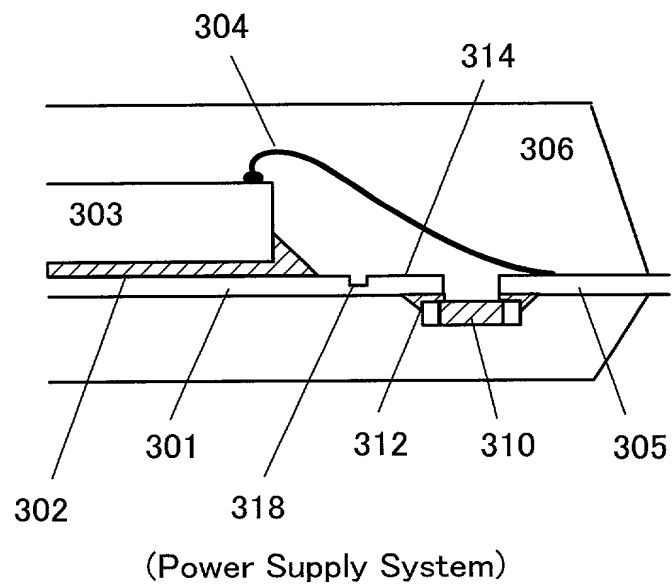
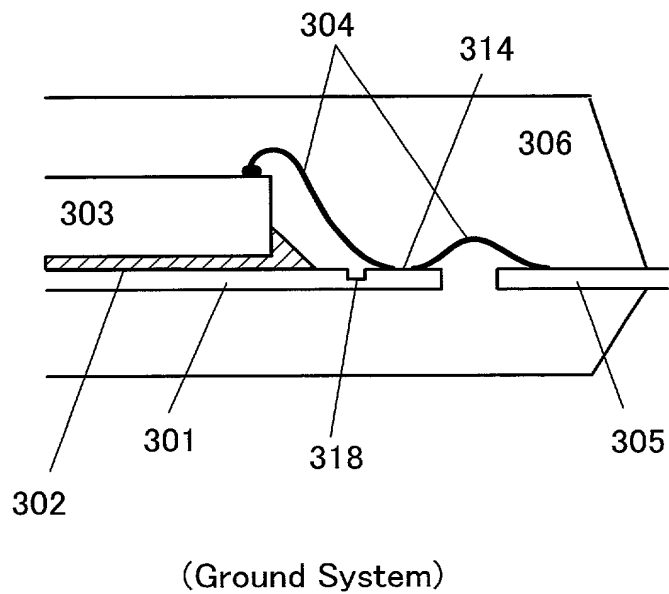
*FIG. 3*

*FIG. 4*

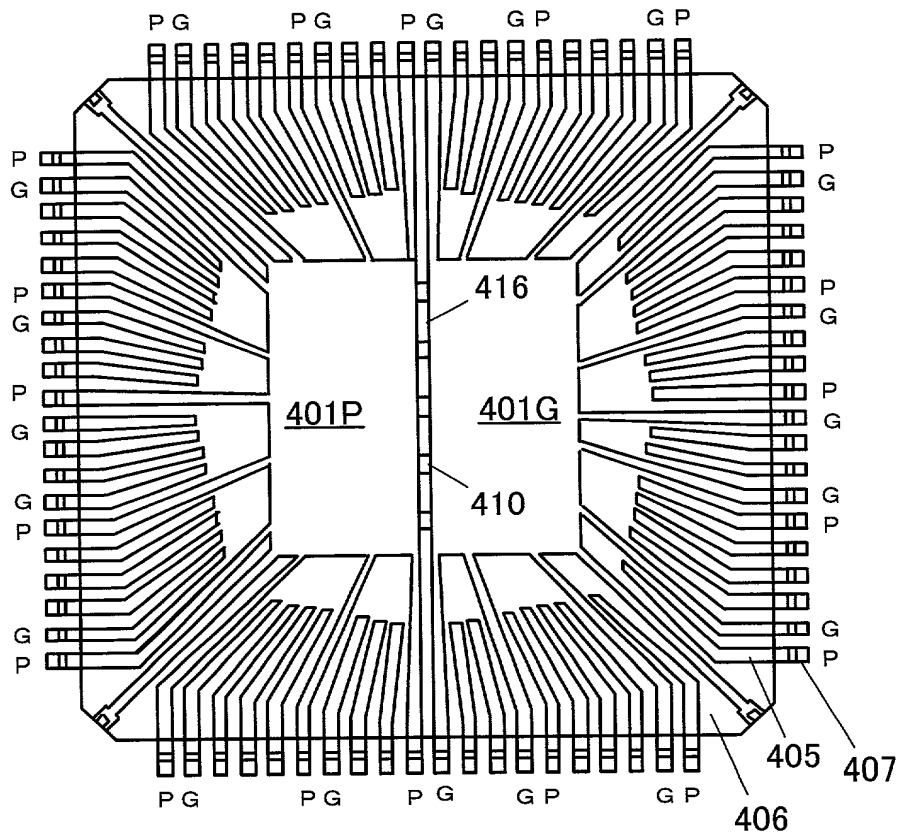
*FIG. 5*

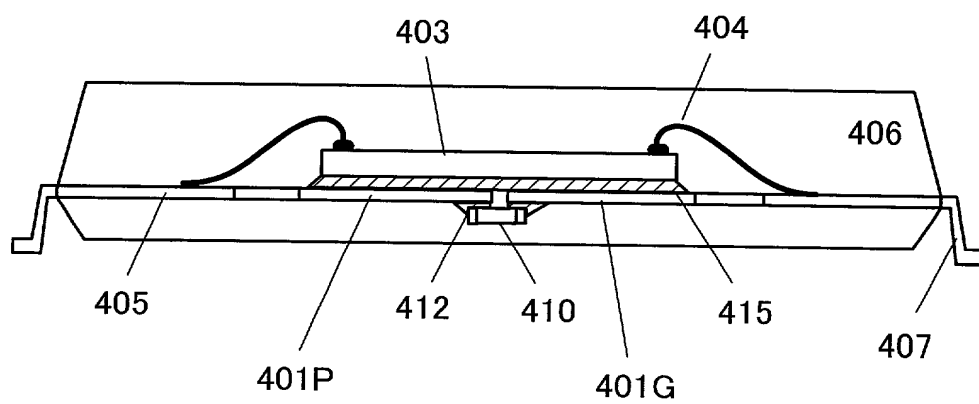
*FIG. 6A**FIG. 6B*

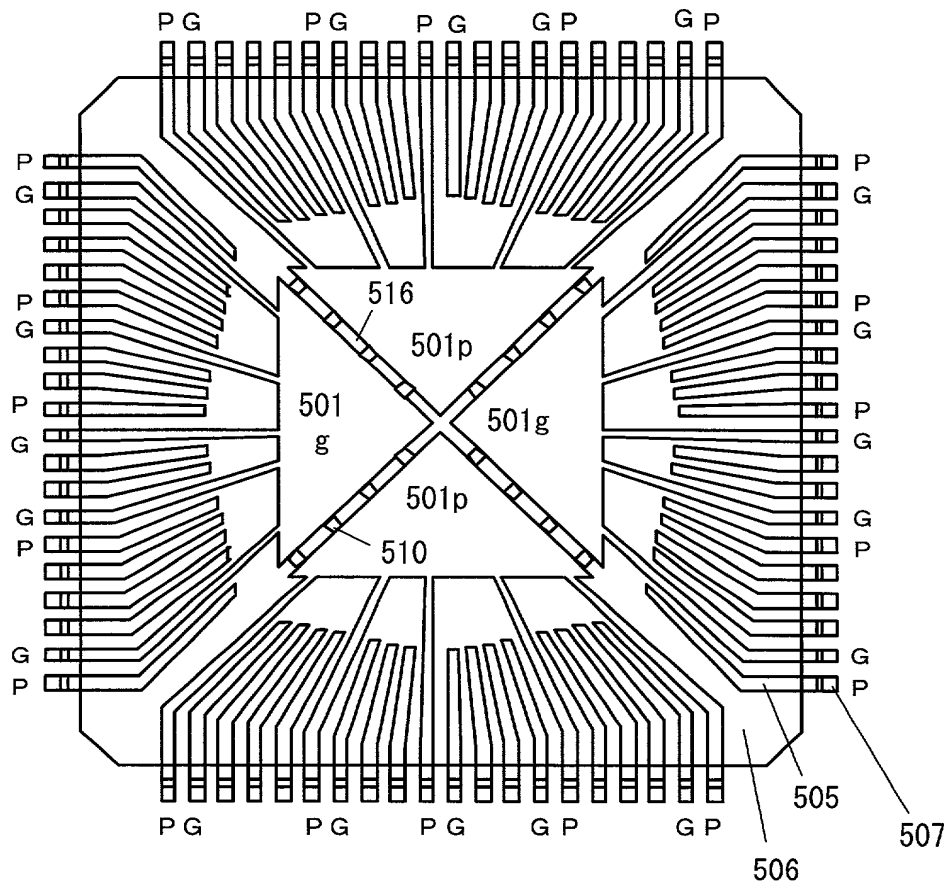
*FIG. 7*

*FIG. 8A**FIG. 8B*

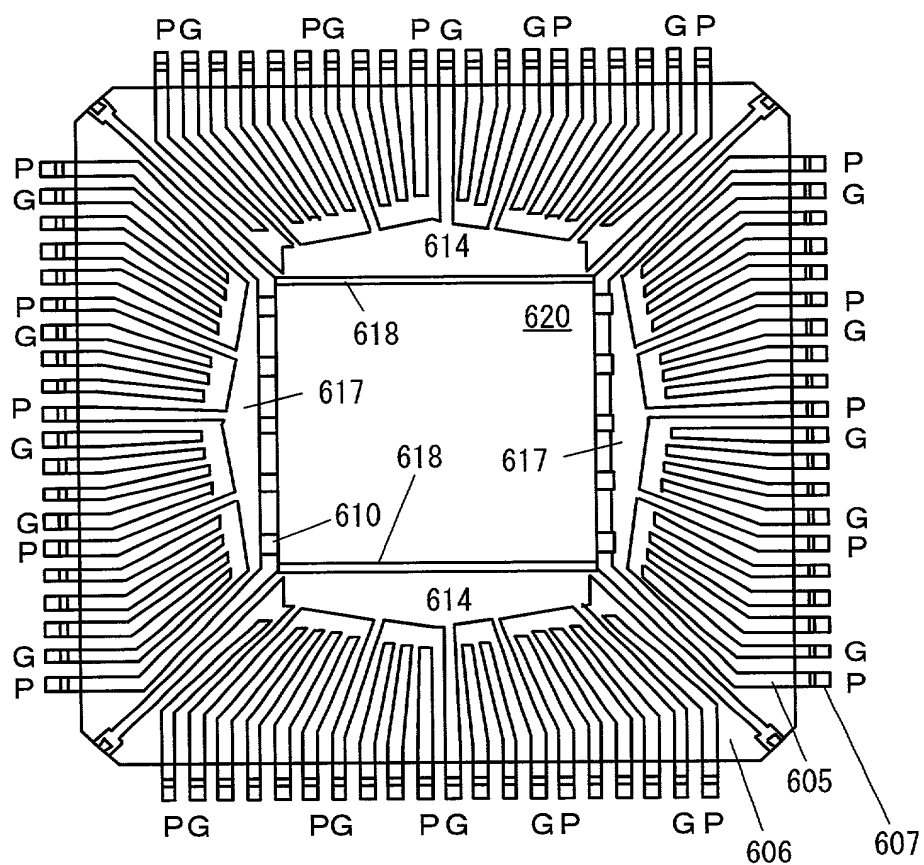


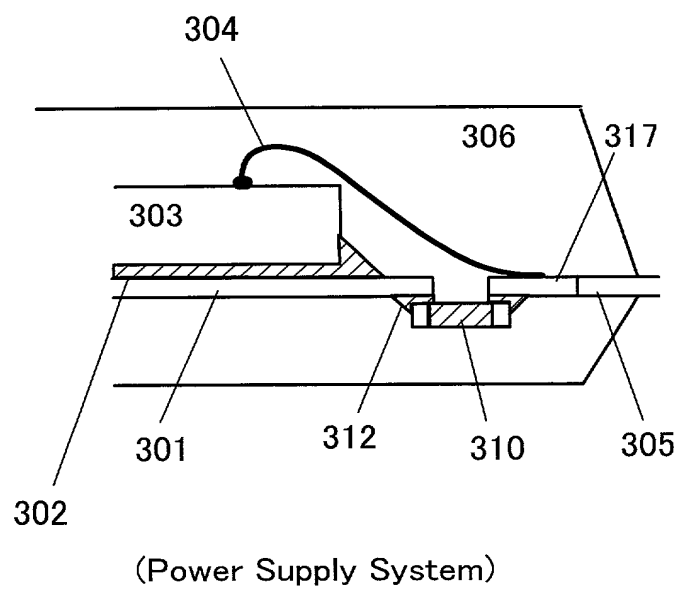
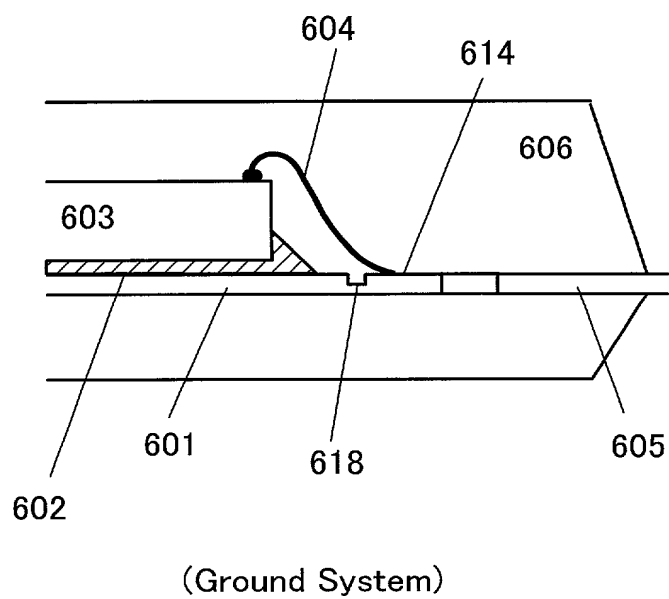
*FIG. 9*

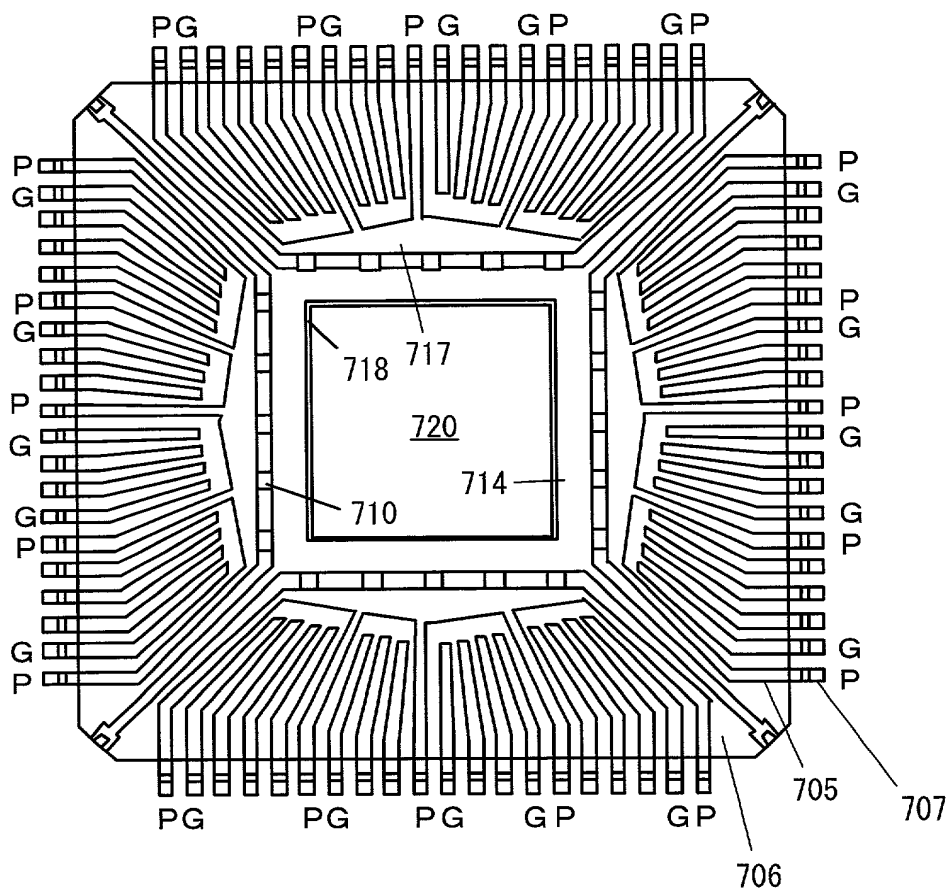
*FIG. 10*

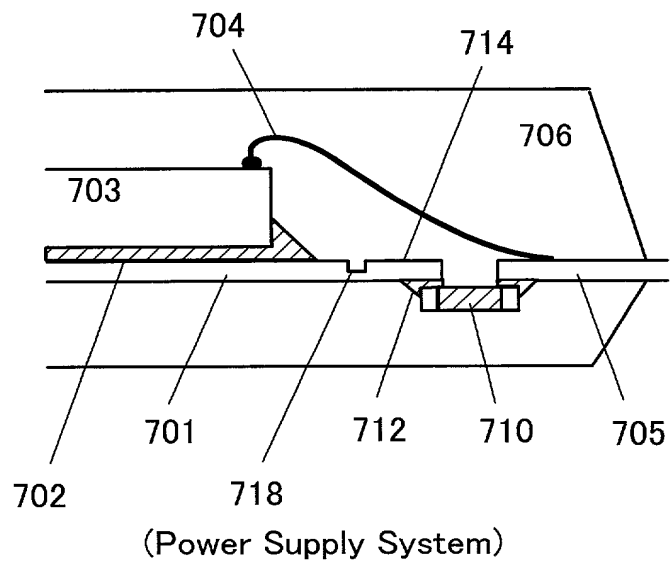
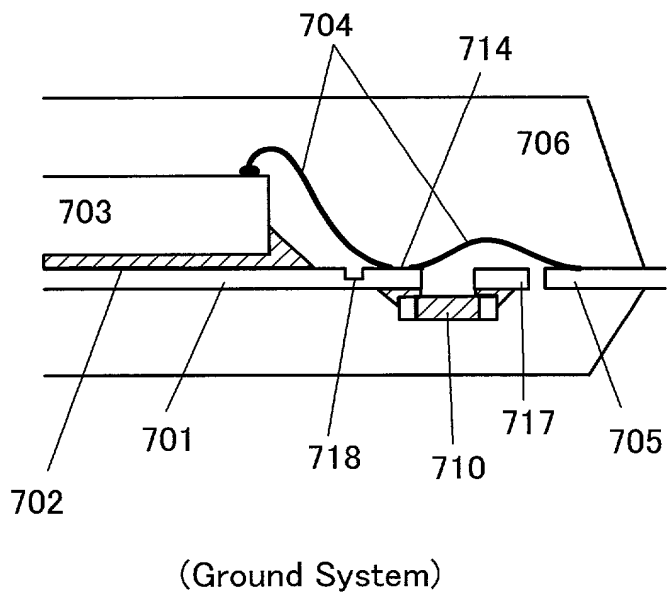
*FIG. 11*

A cross-sectional view of a semiconductor device 500. The device features a substrate 505 with a series of openings 510. A layer 501p, 501g is formed over the substrate, with openings 512 aligned with the substrate openings 510. A central block 503 is positioned on top of the layer 501p, 501g, with electrical contacts 504 and 515 on its top surface. A protective layer 506 covers the top of the device, and a side wall 507 is formed on the right side.

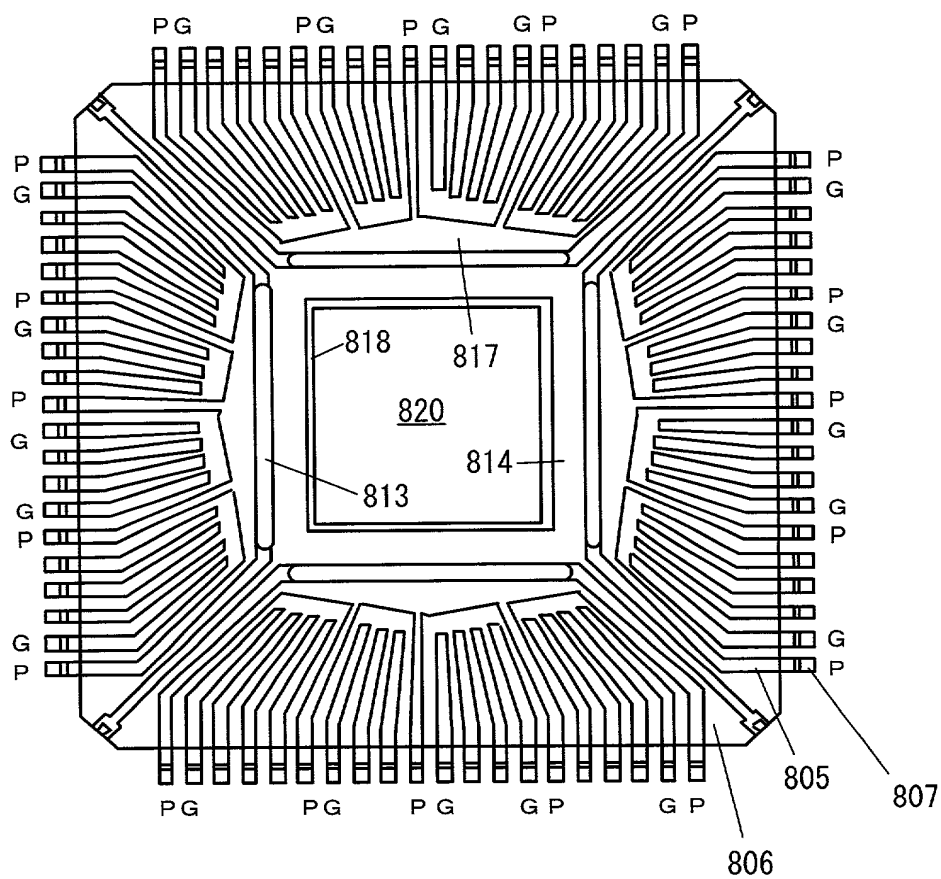
*FIG. 13*

*FIG. 14A**FIG. 14B*

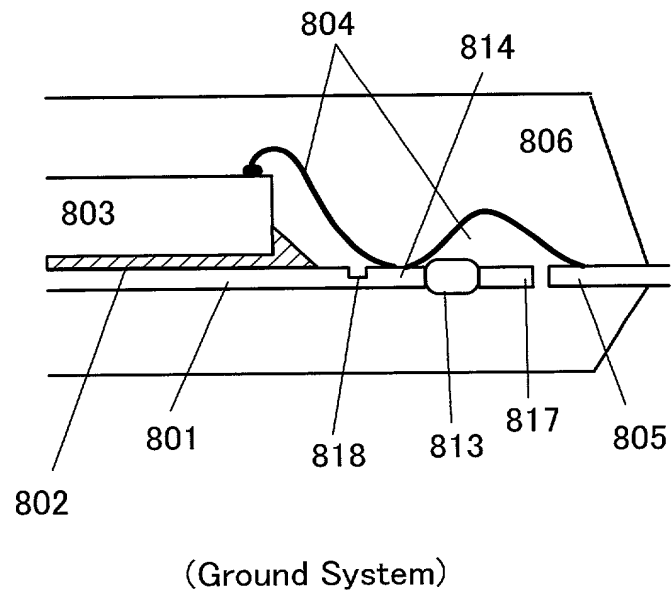
*FIG. 15*

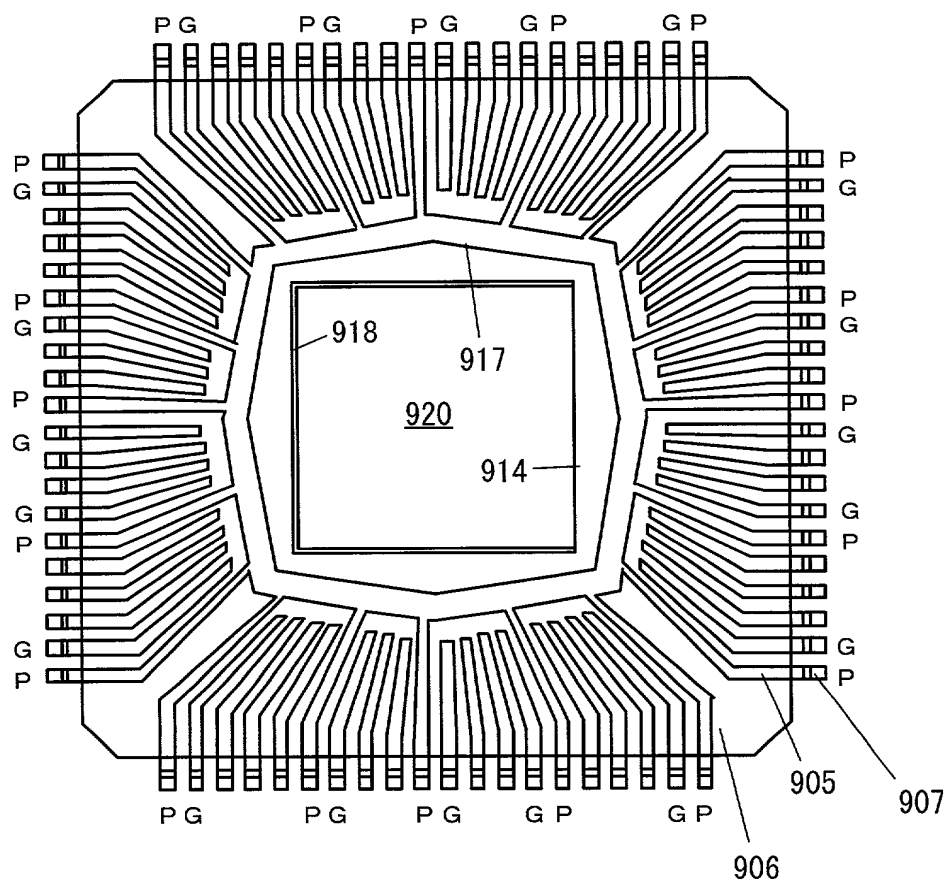
*FIG. 16A**FIG. 16B*

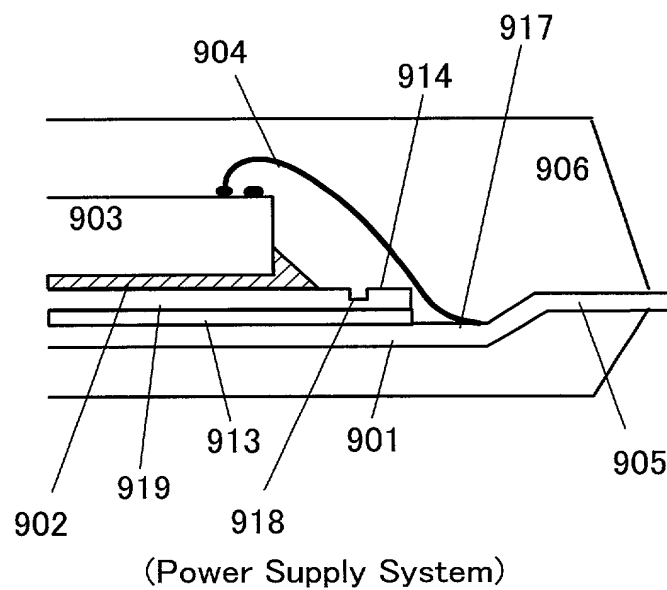
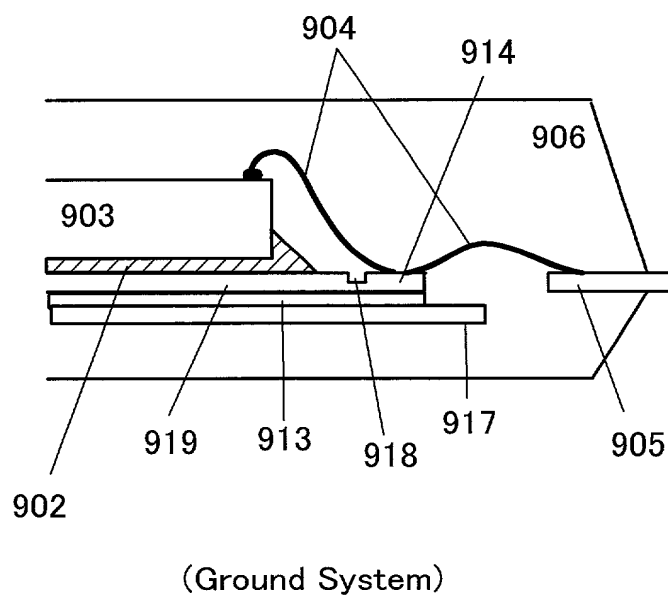


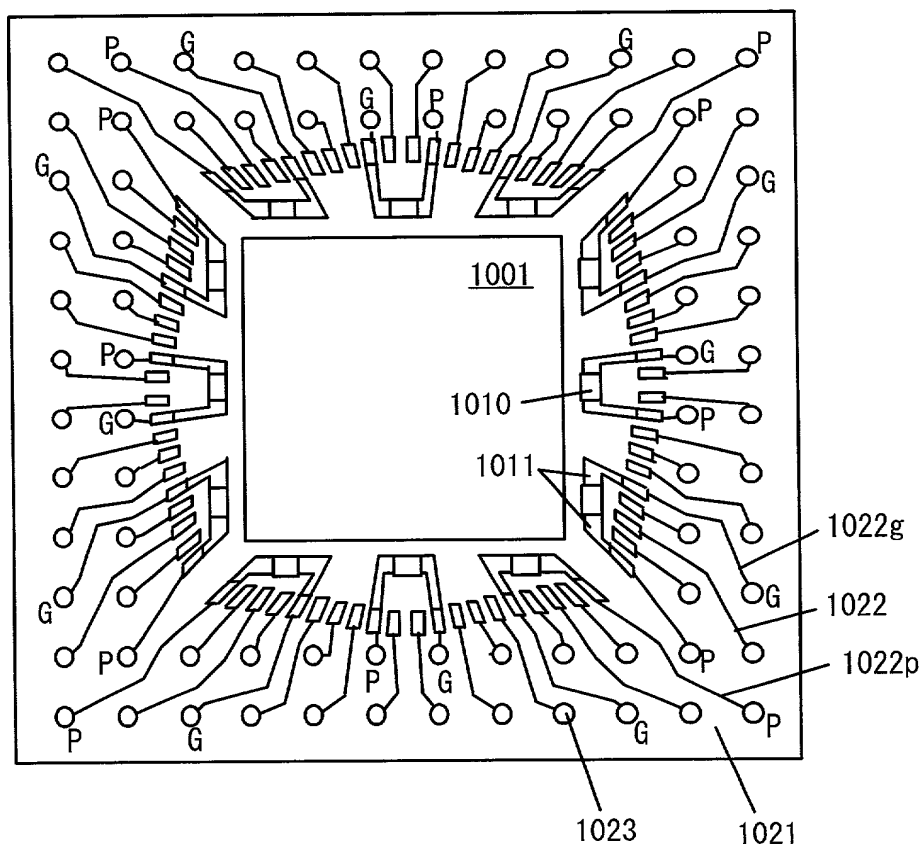
*FIG. 17*

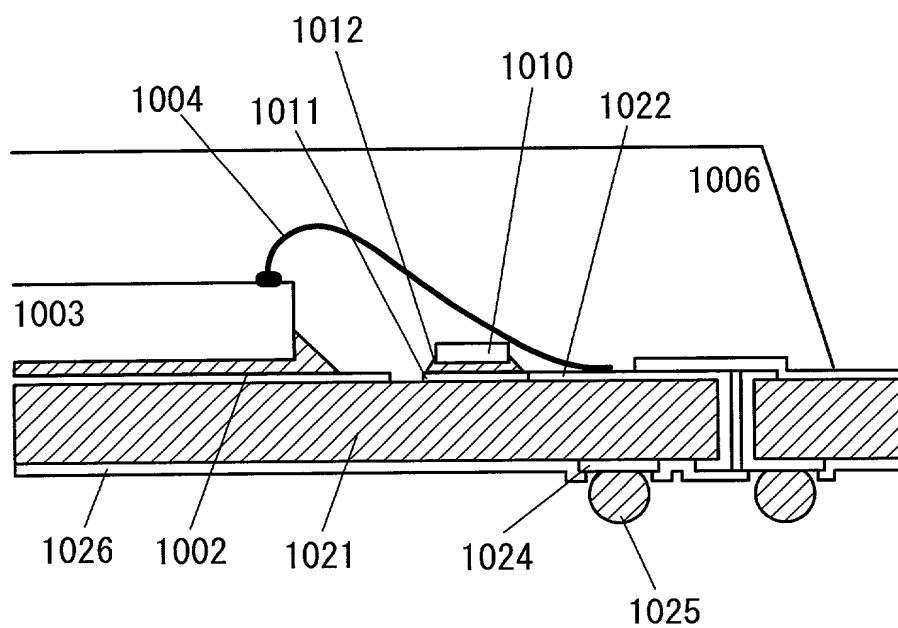
*FIG. 18B*

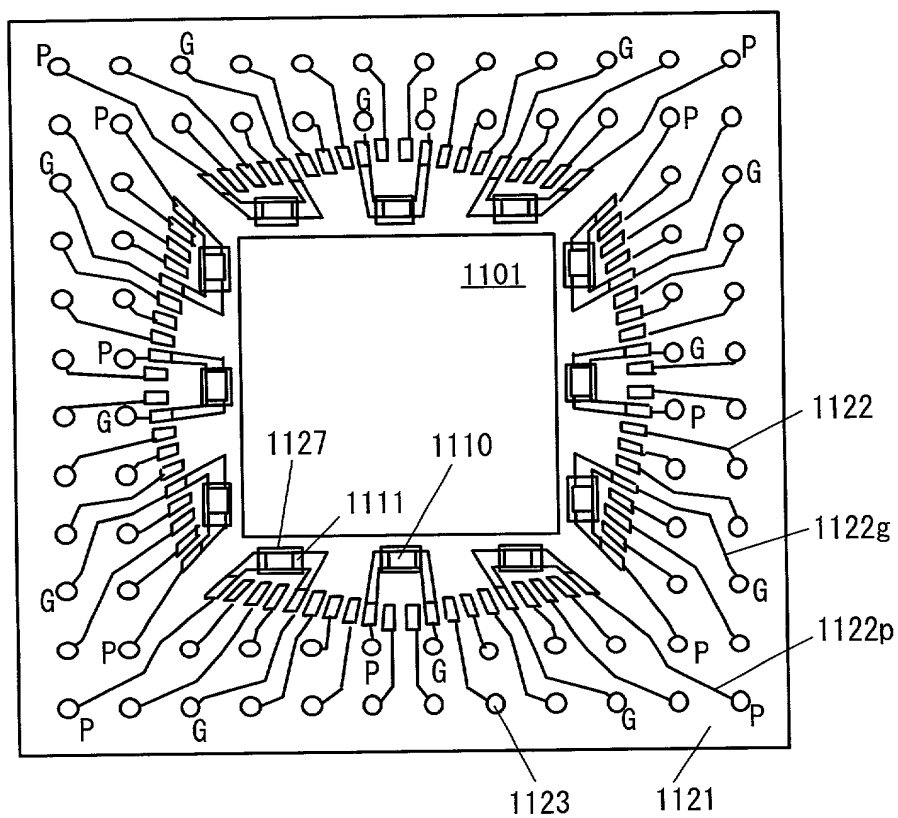


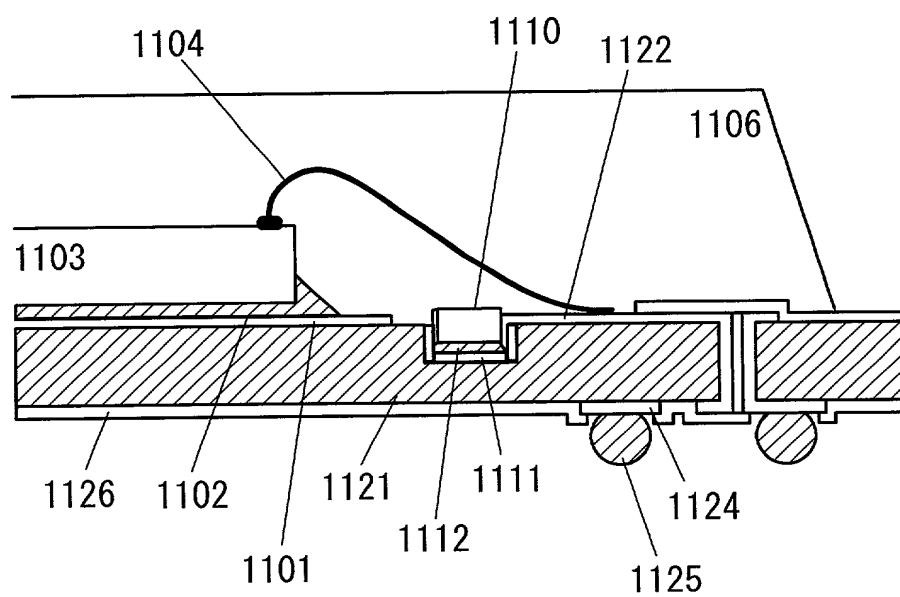
*FIG. 19*

*FIG. 20A**FIG. 20B*

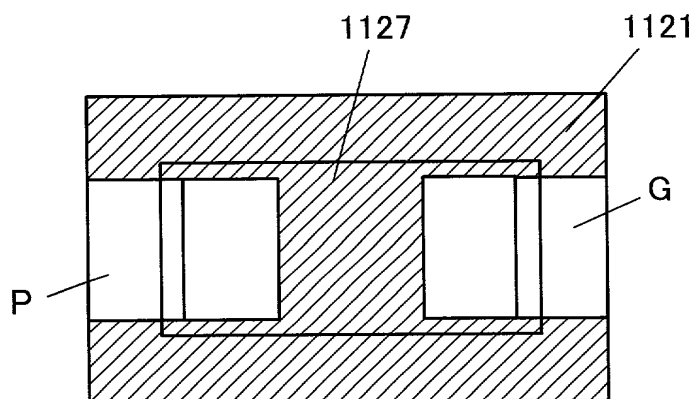
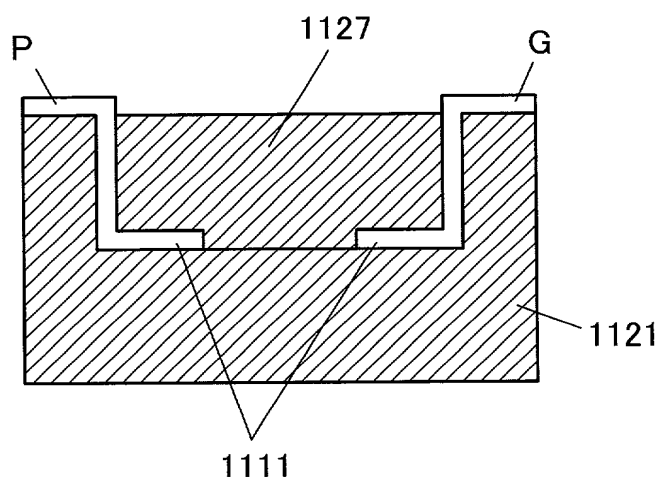
*FIG. 21*

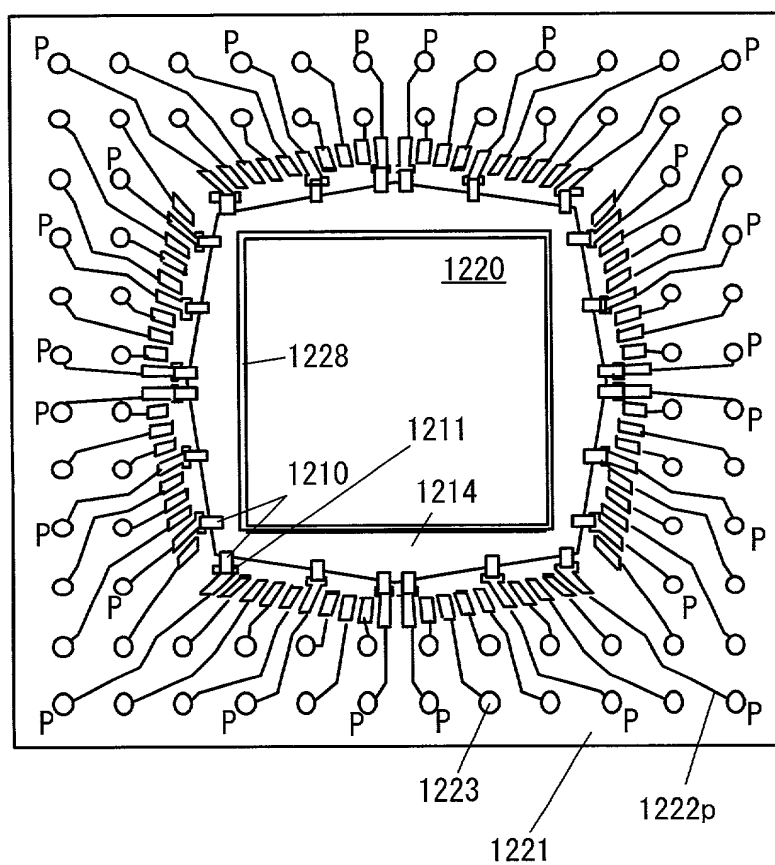
*FIG. 22*

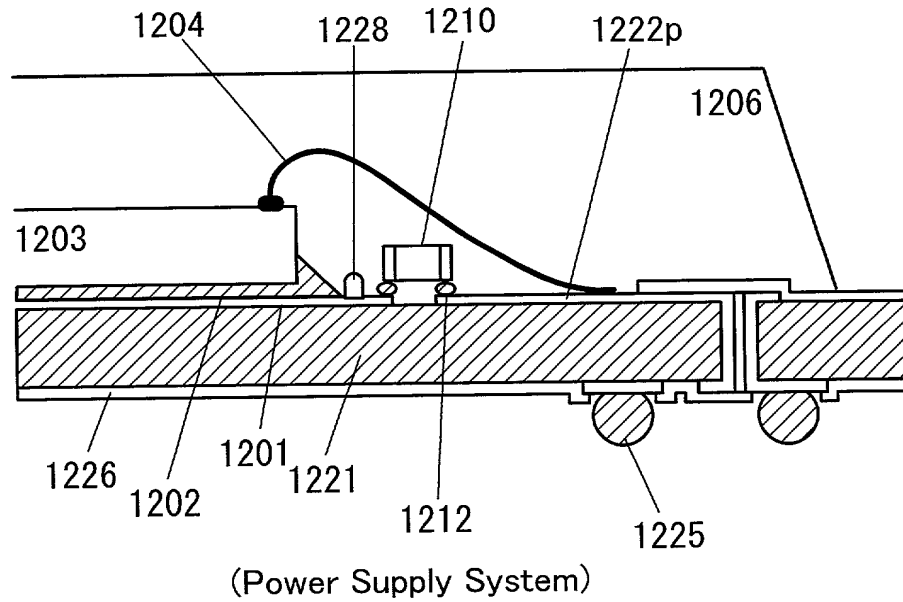
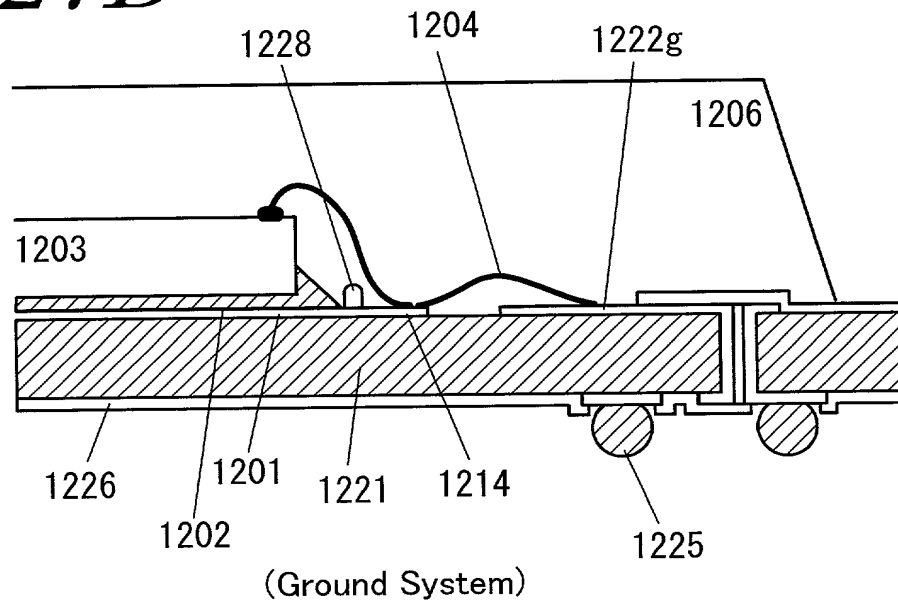
*FIG. 23*

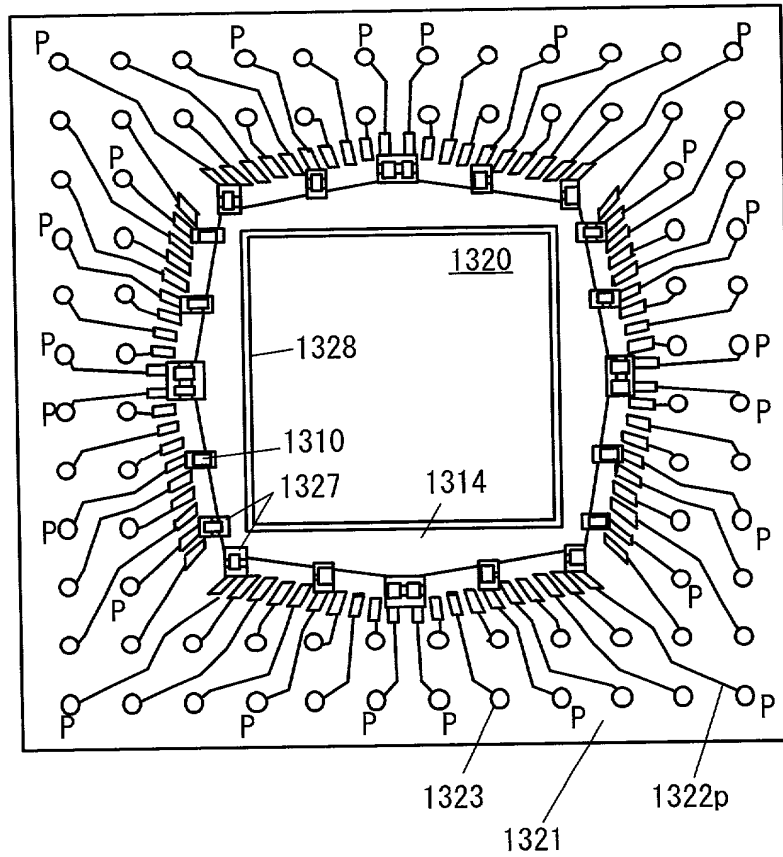
*FIG. 24*

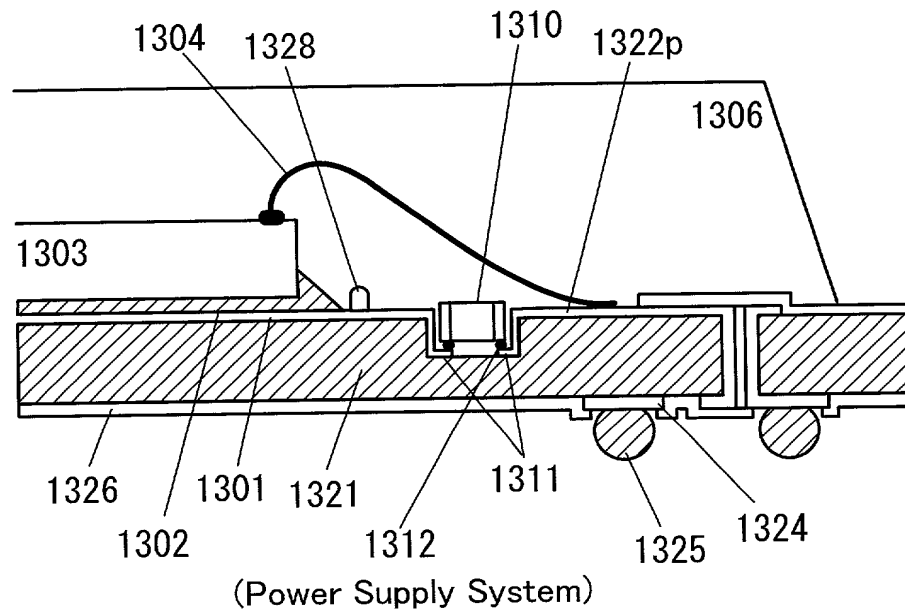
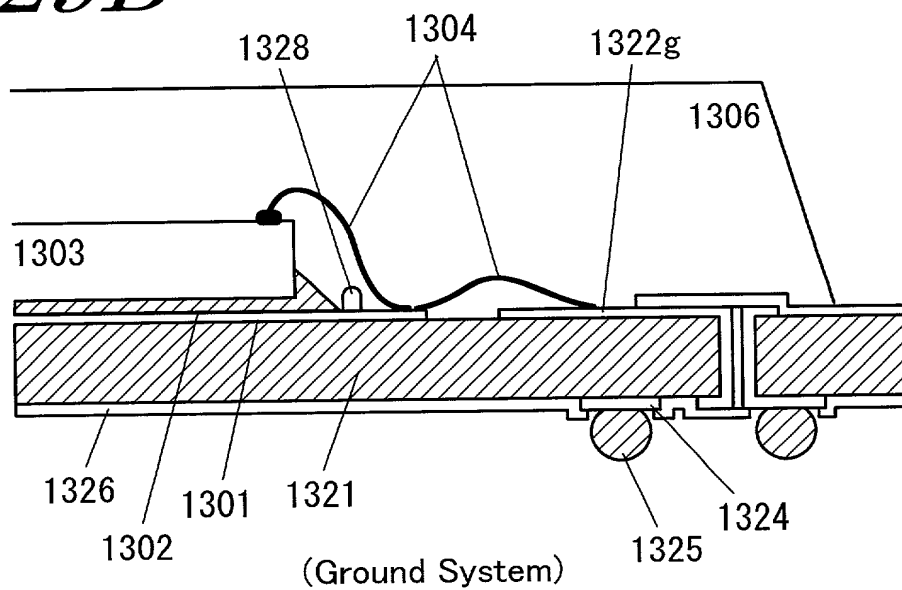


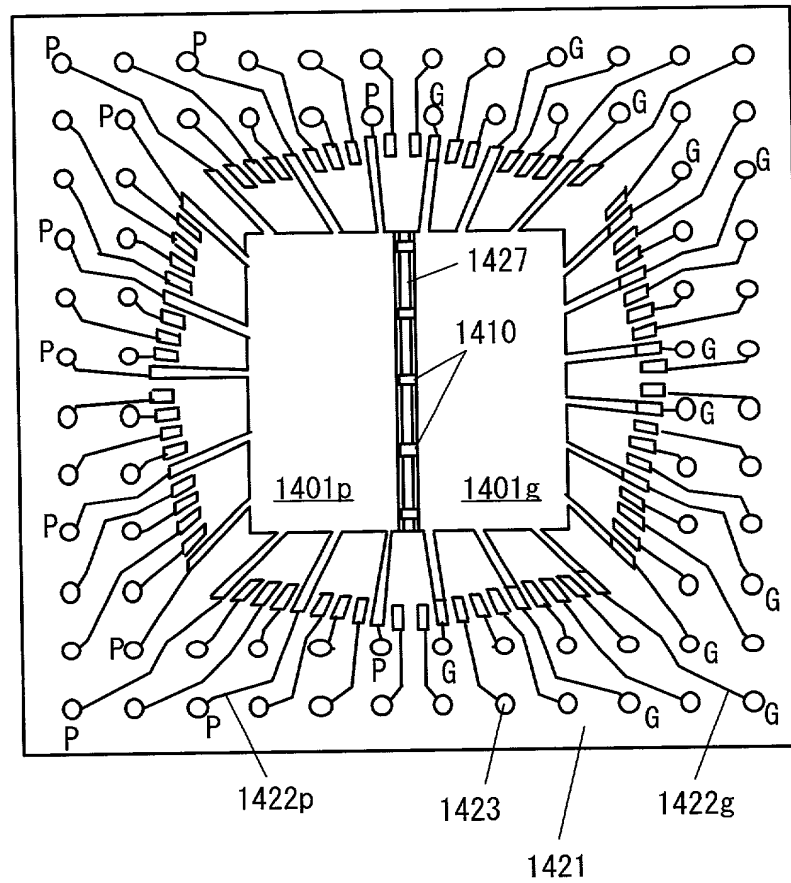
*FIG. 25A**FIG. 25B*

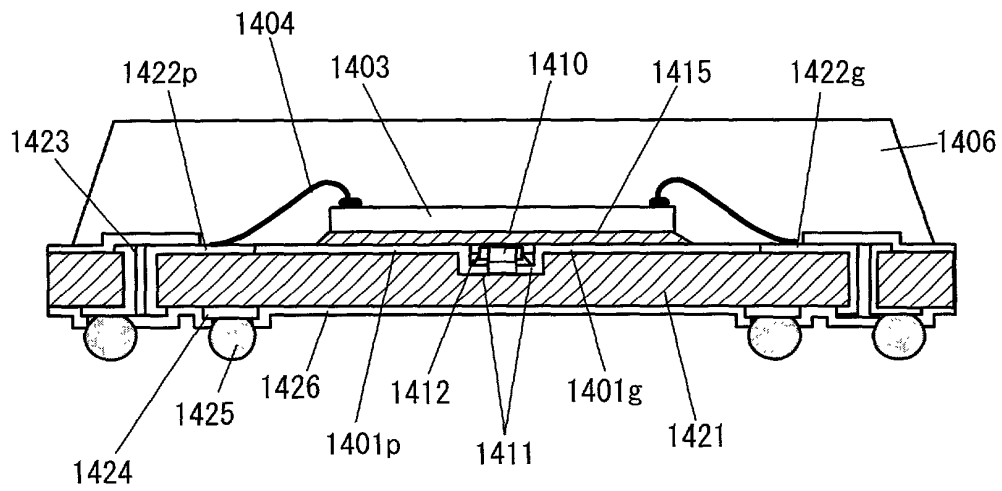
*FIG. 26*

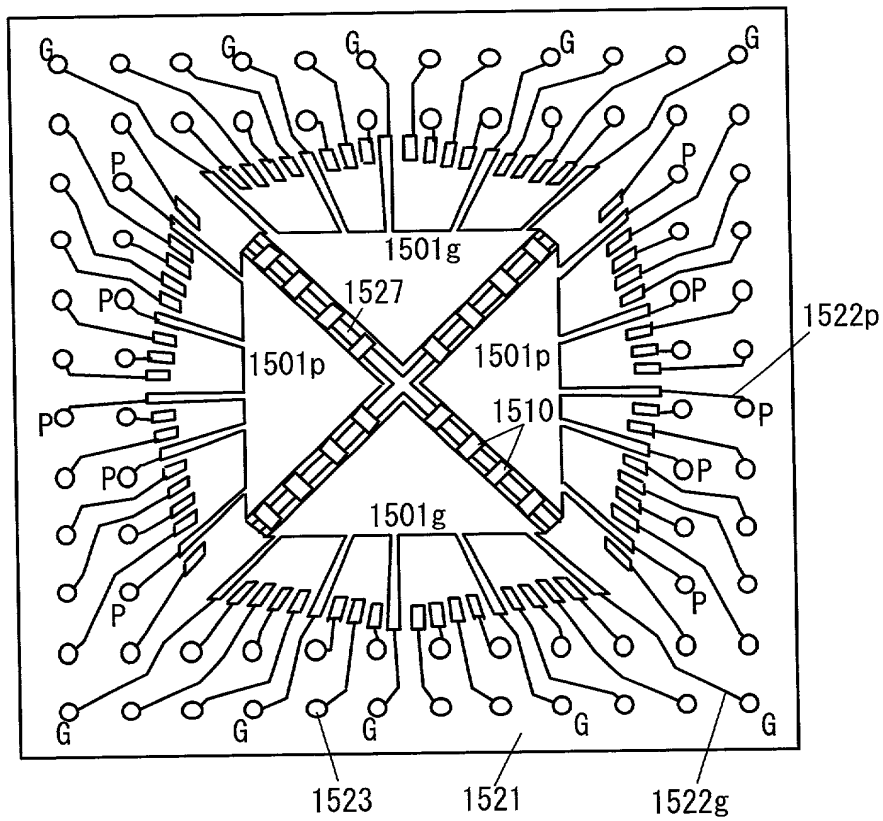
*FIG. 27A**FIG. 27B*

*FIG. 28*

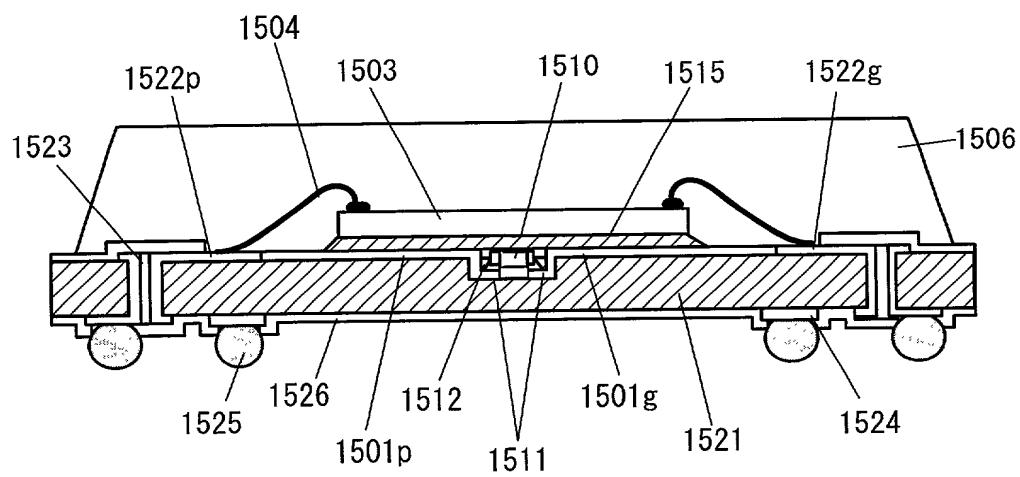
*FIG. 29A**FIG. 29B*

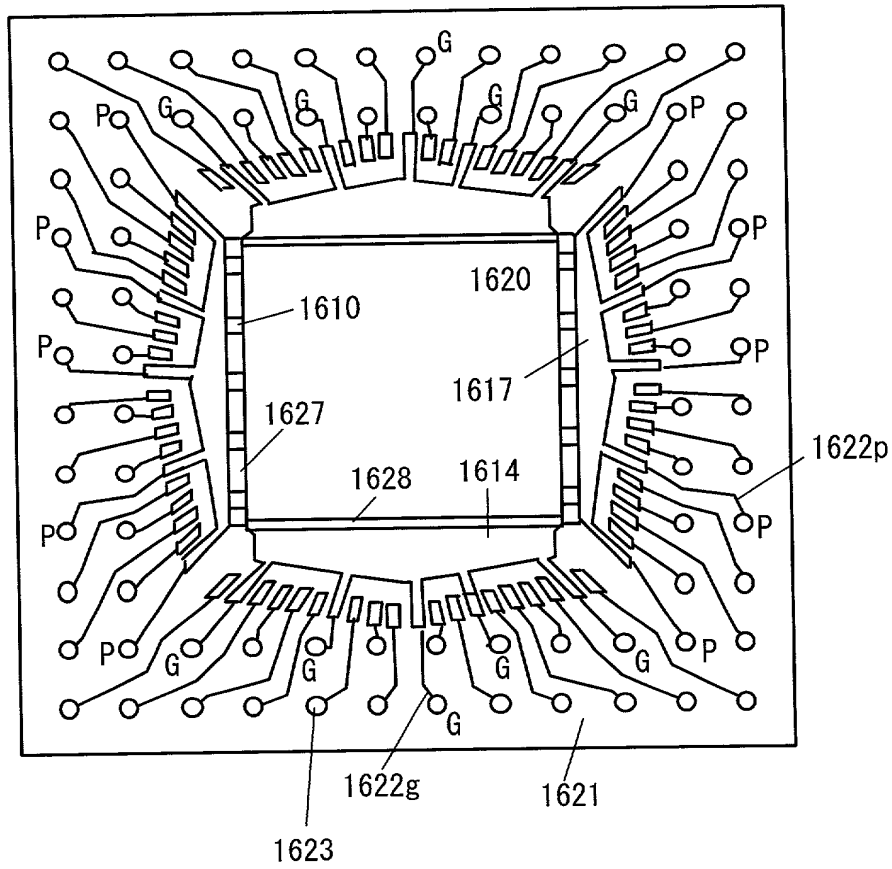
*FIG. 30*

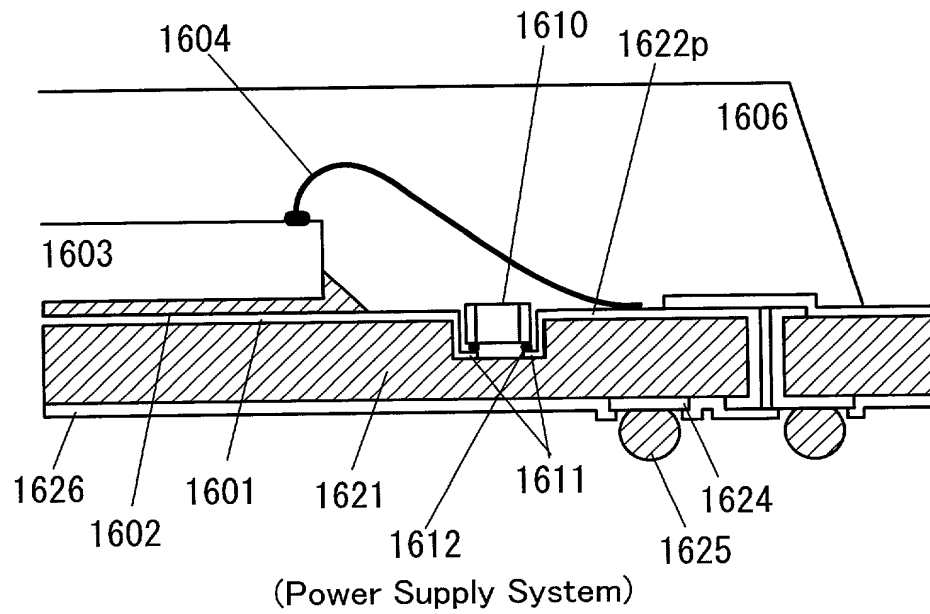
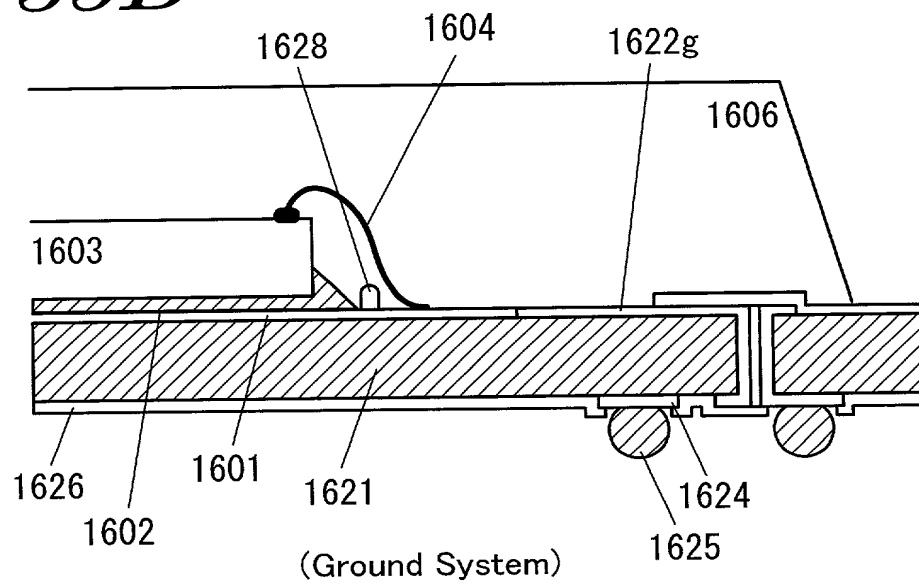
*FIG. 31*

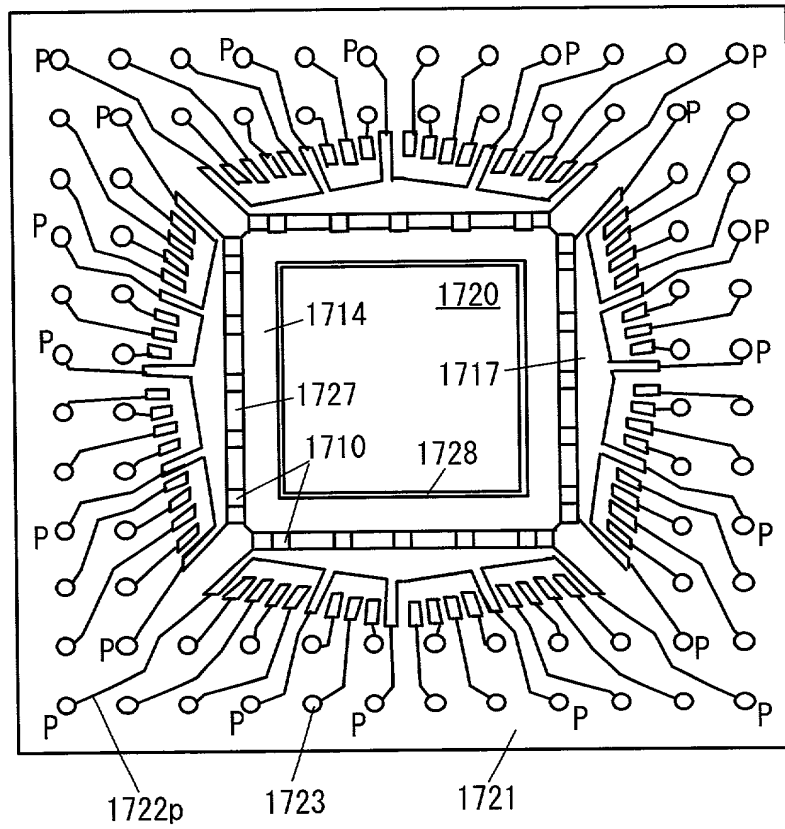
*FIG. 32*



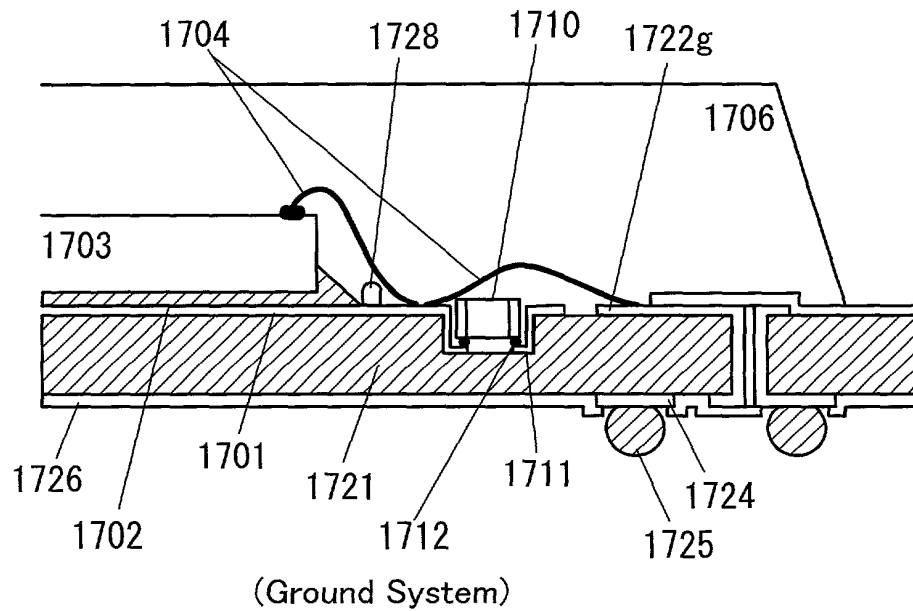
*FIG. 33*

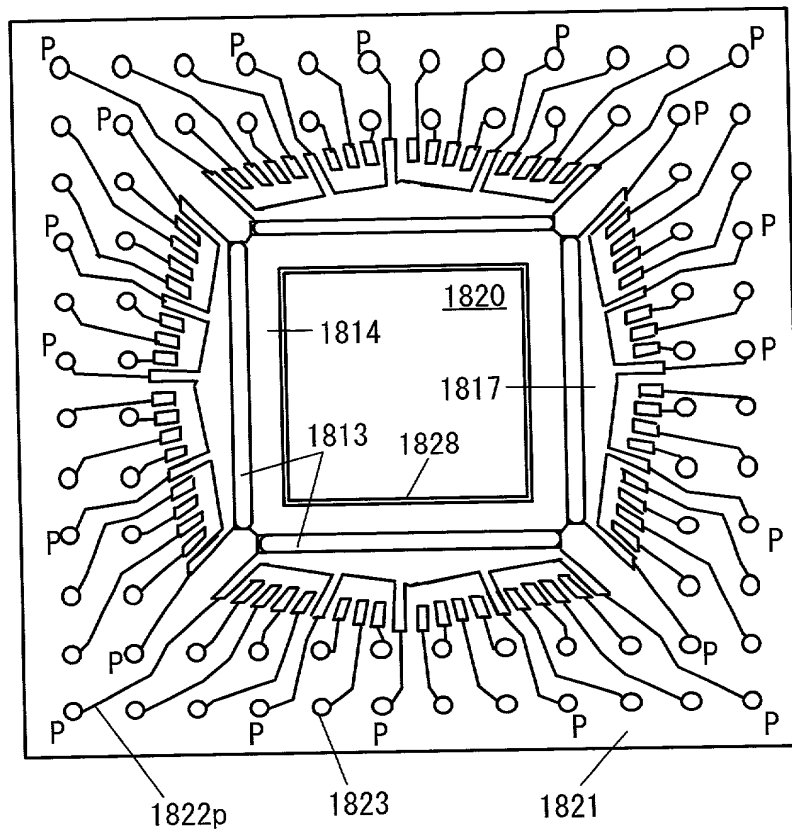
*FIG. 34*

*FIG. 35A**FIG. 35B*

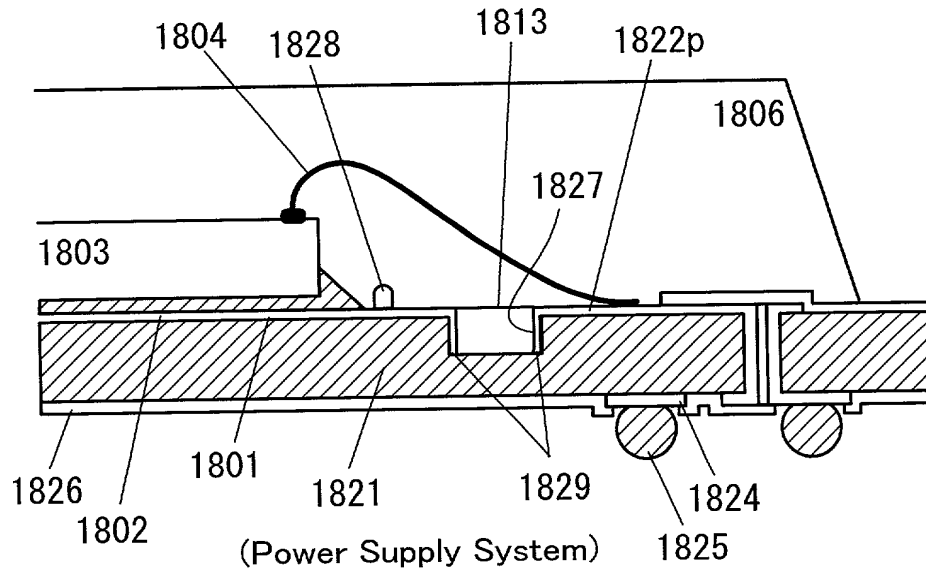
*FIG. 36*

*FIG. 37B*

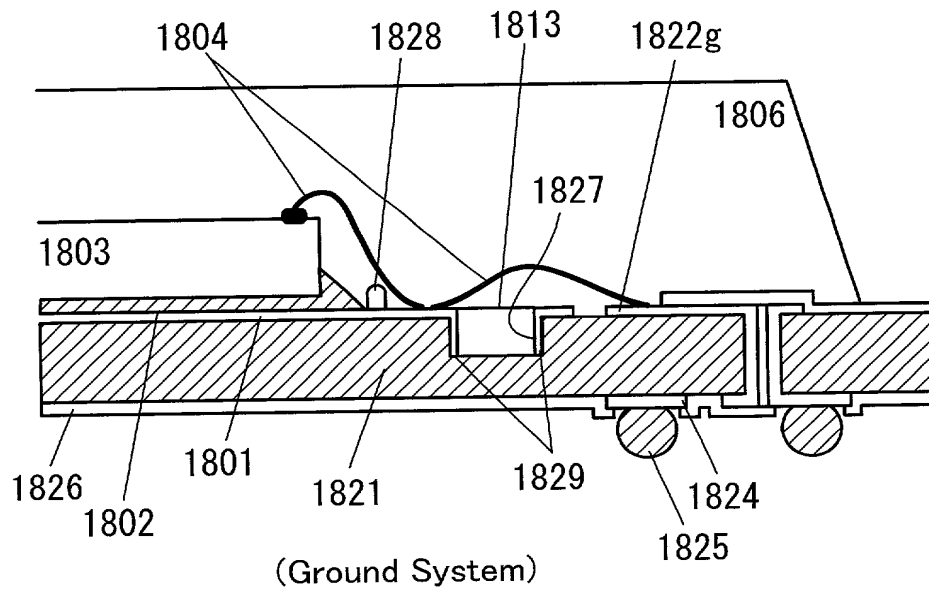


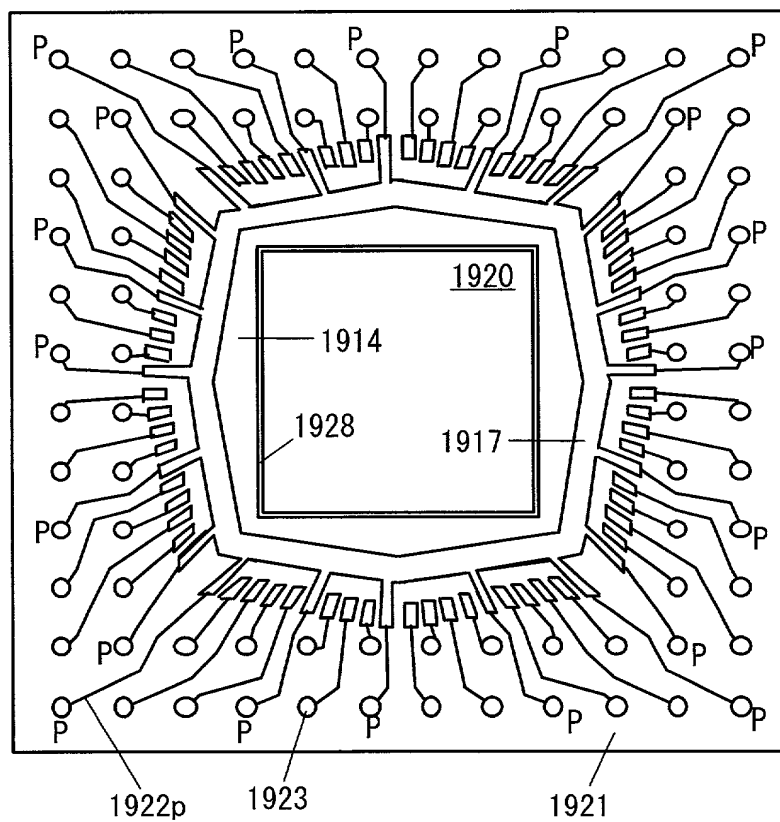
*FIG. 38*

*FIG. 39A*

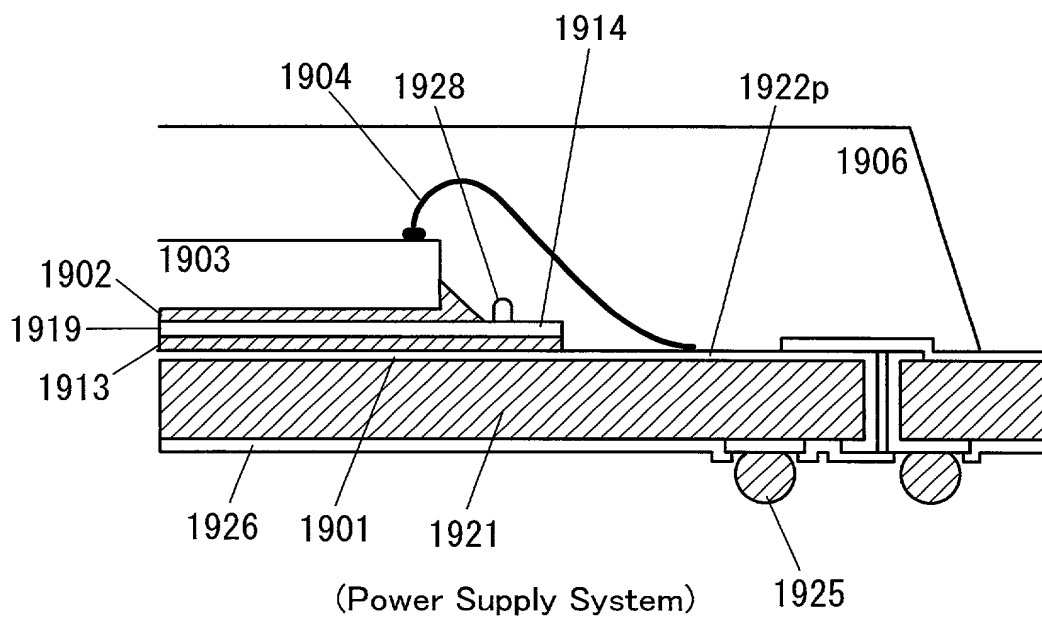


*FIG. 39B*



*FIG. 40*



*FIG. 41A**FIG. 41B*